Letters

Comments on "Modeling of Planar Varactor Frequency Multiplier Devices with Blocking Barriers"

R. J. Hwu

I am compelled to write this comment in disagreement with some information in the paper "Modeling of Planar Varactor Frequency Multiplier Devices with Blocking Barriers" by Lieneweg *et al.* [1]. A precursor to that paper was published in the *Proceedings of the Second International Symposium on Space Terahertz Technology* [2]. It appears to me that some conclusions drawn in this paper are the same as that which were discussed in my thesis (see UCLA thesis 1991). At that time, I raised my concern about the difference of the effective RC time constant between single and two back-to-back connected BIN (Barrier-Intrinsic-N^+) diodes based on high frequency measurement results I had obtained over a period of two years. I also provided an explanation in terms of the behavior of the effective series resistance and capacitance of the back-to-back connected diodes that was not experimentally verified. Lieneweg *et al.* published in two separate publications (see pp. 272–277, "Design of Planar Varactor Frequency Multiplier Devices with Blocking Barriers," *Proceedings of the Second International Symposium on Space Terahertz Technology* and pp. 840–842, "Modeling of Planar Varactor Frequency Multiplier Devices with Blocking Barriers," Vol. 40, no. 5, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES) the same discussions on the behavior of the series resistance and capacitance. However, I have conducted a series of measurements for determining the effective series resistance, capacitance and RC time constant of the back-to-back connected diodes since that time. These measurements illustrtae the behavior of the effective series resistance and capacitance which are somewhat different than what I assumed in my thesis and what Lieneweg *et al.* published in [1] and [2]. These differences are as follows:

I. Capacitance-Voltage Characteristic and Voltage Distribution

The C-V characteristics measured from single and back-to-back diodes have been studied. From these results, the capacitance from the back-to-back diode is different from what was discussed in [1] and [2]. Specifically, the maximum capacitance, $C_{\max,b}$, of the back-to-back diode is approximately half of the zero-bias capacitance of the single diode, $C_{o,s}$, instead of half of $C_{\rm bar}$, where $C_{\rm bar} = \epsilon_{\rm bar} A/d_{\rm bar}$ as stated in [1] and [2]. The minimum capacitance, $C_{\min,b}$, of the back-to-back diode is approximately $1/(1/C_{o,s}+1/C_{\min,s})$, instead of $1/(1/C_{\min,s}+2/C_{\rm bar})$ as stated in [1] and [2], where $C_{\min,s}$ is the capacitance of a single diode under a large reverse bias for which the epilayer is fully depleted. In other words, when one diode has a capacitance value of $C_{{\rm bias},s}$, the other diode will always have a capacitance value of $C_{o,s}$. Thus, when applying a dc bias to the back-to-back diode, one diode will be reverse biased while the other diode will be at zero bias. Therefore, the dc bias voltage is completely distributed on one diode and no voltage is distributed on the other diode when a dc bias is applied to the back-to-back diode.

TABLE I
Effective Series Resistances and Capacitances of Single and Back- to-Back Diodes of the Same Varactor Structure Determined From High-Frequency Impedance Measurements

SMALL-SIGNAL OPERATION

	Single (reverse biased)	Back-to-Back (zero bias)
R	$\gtrsim 0.5R_s$	$2R_s$
C	$\gtrsim C_{\rm bias} \approx \frac{C_{\max,s}+C_{\min,s}}{2}$	$\frac{1}{2}C_{o,s}$

LARGE-SIGNAL OPERATION

	Single (reverse biased)	Back-to-Back (zero bias)
R	$\approx 0.5R_s$	R_s
C	$\approx \frac{C_{\max,s}+C_{\min,s}}{2}$	$\frac{C_{\min,s}\,C_{o,s}}{C_{\min,s}+C_{o,s}} \approx C_{\min,s}$

II. Effective Series Resistance

To determine the effective series resistance of the back-to-back diode, a series of high-frequency impedance measurements were performed on single and back-to-back diodes. The results from these measurements are summarized and listed in Table I. It should be pointed out that all the measurements on the back-to-back diode were performed at zero bias to preserve the symmetrical C-V characteristic. The effective series resistance of the back-to-back diode is $\approx 2R_s$ for small-signal operation and decreases at large-signal operation. The effective series resistance value of the back-to-back diode becomes $\approx R_s$ for very large-signal operation. Varactor diodes are usually reverse biased to avoid current flow during frequency multiplication operation. The effective series resistance value of a reverse-biased single diode was also measured and listed in Table I for comparison. The effective series resistance of a biased single diode is $< R_s$ for the small-signal case and decreases at large-signal operation. The effective series resistance value is close to 0.5 R_s at very large-signal operation, which is roughly the average of the series resistance of a strongly forward- and reverse-biased diode. It should be noted here that the effective series resistance value for the back-to-back diode operation decreases with increasing RF pump level. The effective resistance of a single diode, however, stays roughly the same with increasing RF pump level.

It should be pointed out that the high frequency behavior of the back-to-back diode is similar to the low frequency behavior which was discussed in the above section. When applying a RF signal to the back-to-back diode, the pump amplitude is distributed on one diode completely and no pump amplitude is distributed on the other diode. In other words, one diode is always reverse biased while the other diode is always zero-biased when applying a RF signal to the back-to-back diode.

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III. Effective Capacitance

The effective capacitance values of both single and back-to-back diodes from the high-frequency impedance measurements are also listed in Table I. The effective capacitance value of the back-to-back diode under small-signal conditions is equal to 0.5 $C_{o,s}$ which is similar to that obtained from the C-V measurements. The effective capacitance value of a reverse-biased diode under small-signal operations is close to the expected capacitance at the bias point. Since the diode is usually biased at the middle of the C-V nonlinearity region, the capacitance value at this bias point is close to the average value of the maximum and minimum capacitance of the device, i.e., $(C_{\max,s} + C_{\min,s})/2$. The effective capacitance value of a reverse-biased diode under large-signal operation is between $C_{\max,s}$ and $C_{\min,s}$. This effective capacitance value is determined by the C-V characteristic of the diode and is also very close to the average of the maximum and minimum capacitance of the device, i.e., $(C_{\max,s} + C_{\min,s})/2$. However, the effective capacitance value of the back-to-back diode under large-signal operation is equal to $1/(C_{o,s} + 1/(C_{\min,s})$ which is very close to $C_{\min,s}$ when the capacitance ratio $(C_{o,s}/C_{\min,s})$ is large. It should also be pointed out that while the effective capacitance value of the back-to-back diode decreases with increasing RF pump level, the effective capacitance value of a reverse-biased single diode remains roughly constant with increasing RF pump level. This result is not surprising in the single diode operation, as the effective capacitance value is roughly the average capacitance during the RF pump cycle; in the back-to-back operation, one diode is always zero-biased and the other diode is always reversed biased. The effective capacitance of the back-to-back diode is, therefore, determined by the capacitance of the reverse-biased diode and decreases with increasing RF pump level. This high frequency C-V nonlinearity is expected from the low-frequency C-V behavior study. This result, again, demonstrates that when the epilayer of one diode is depleted by a reverse bias, the other diode is always zero biased; this result is different from that was published by Lieneweg *et al.* [1], [2].

IV. Cut-Off Frequency and RC Time Constant (Transit Time)

Based on the above results, the effective RC time constant of the back-to-back diode decreases at a higher rate with increasing RF pump level than that of a single diode. The effective RC time constant of the back-to-back diode is higher than that of a single diode under small-signal operation and slowly approaches that of a single diode under large-signal operation. Therefore, the effective cut-off frequency of the back-to-back diode configuration is lower than that of a single diode under small-signal operation and approaches that of a single diode under large-signal operation. This fact was not pointed out in the two publications by Lieneweg *et al.*, [1], [2].

Based on the argument that Lieneweg *et al.* have made for the behavior of the series resistance and capacitance in their two publications [1], [2], one diode is at reverse bias while the other diode is at forward bias when applying a RF signal to two back-to-back diodes which has been experimentally demonstrated to be wrong. The large-signal analysis results presented in these papers (if they were based on this assumption) are invalid since the assuming C-V nonlinearity and effective RC time constant are different from the real behavior of two back-to-back connected diodes. The large-signal nonlinear-circuit analysis program of Siegel *et al.* [3] has been used to calculate the optimum tripling efficiency of the back-to-back diode with these two different types of voltage distributions, i.e., in one case, one diode is reverse biased while the other diode is always at zero bias (experimental observation), in the other case, one diode is reverse biased while the other diode is forward biased (published by Lieneweg *et al.* [1], [2]). The optimum tripling efficiency of a back-to-back diode with the voltage distribution published by Lieneweg *et al.* is higher than (by roughly 10%) it really should be. The optimum tripling efficiency is also higher than it really is due to the stronger C-V nonlinearity from the voltage distribution published by Lieneweg *et al.* [1], [2].

References

[1] U. Lieneweg, T. Tolmunen, M. Frerking, and J. Maserjian, "Modeling of planar varactor frequency multiplier devices with blocking barriers," *IEEE Trans. Microwave Theory Tech.*, vol. 40, no. 5, pp. 839–845, May 1992.

[2] ——, "Design of planar varactor frequency multiplier devices with blocking barriers," *Proc. Second Int. Symp on Space Terahertz Technology*, 1991, pp. 270–284.

[3] P. H. Siegel, A. R. Kerr, and W. Huang, "Topics in the optimization of millimeter-wave mixers," NASA Tech. Paper 2287, 1984.

Reply to Comments on "Modeling of Planar Varactor Frequency Multiplier Devices with Blocking Barriers"

U. Lieneweg, T. Tolmunen, M. A. Frerking, and J. Maserjian

In replying to the above comments on our paper [1] made by R. J. Hwu we wish to stress the following points:

I. C-V Characteristics

a) For the kind of nearly rectangular characteristics to which we are referring, cf. Fig. 4 in [1], the difference between the zero-bias capacitance of a single diode $C_{o,s}$ and the barrier capacitance $C_{\rm bar}$ is immaterial.

b) Our formula for the minimum capacitance of the back-to-back diode has been misquoted. In Eq. (6) of [1] $C'_{\min}$ means the minimum capacitance of the drift layer, not that of a single diode.

c) The statement that "the dc bias voltage is completely distributed on one diode and no voltage is distributed on the other diode" is an *approximation* that may be explained by nonideally blocking barriers with large forward conduction.

It is not true in general as we have verified for good heterojunction barriers. Even for nonideal barriers, like the Mott-barrier, the capacitive behavior should extend to larger forward biases at near-millimeter-wave frequencies. Thus we insist that our formula is for the practical purposes of our application correct.

II. Effective Series Resistance

The measurement of the effective series resistance by an impedance bridge may give useful information if carried out carefully and interpreted cautiously:

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a) The measurement should be of the 5-terminal type in order to exclude parasitic resistances and capacitances.

b) Standard use of a bridge is to measure linear parameters. For the large-signal application to a highly nonlinear device the applied and resulting waveforms must be considered. Our tripler simulations assumed sinusoidal *currents* at the fundamental and the third harmonic. Because of $dV_c/dt = i/C$, the ratio of the time spent at a large capacitance $\approx C_{\max}$ to the time spent at a small capacitance $\simeq C_{\min}$ is larger than the time ratio obtained for an impressed sinusoidal *voltage*. The same time ratio applies to the weighting of R. Not knowing the waveforms in the bridge, we consider the large-signal rsults communicated in Hwu's "Comments" as qualitative only with the possibility that the effective series resistances under current drive may be somewhat higher, as assumed in [1].

References

[1] U. Lieneweg, T. J. Tolmunen, M. A. Frerking, and J. Maserjian, "Modeling of planar varactor frequency multipliers with blocking barriers," *IEEE Trans. Microwave Theory Tech.*, vol. 40, no. 5, pp. 839–845, May 1992.

Comments on "Optimum Noise Measure Terminations for Microwave Transistor Amplifiers"

Ji-Chyun Liu, Sheau-Shong Bor, and Po-Chiang Lu

In the above paper [1], the authors have introduced a graphical method of obtaining circles of constant noise measure in the source reflection coefficient plane to achieve an optimal design of microwave transistor amplifiers.

The authors presented incorrect expressions in (5), and (6) on p. 1255. These are typographical errors. The correct expressions should be

$$F = F_{\min} + 4r_n \frac{|\Gamma_s - \Gamma_{\text{on}}|^2}{(1 - |\Gamma_s|^2)|1 + \Gamma_{\text{on}}|^2} \tag{5}$$

$$G_a = \frac{|S_{21}|^2(1 - |\Gamma_s|^2)}{(1 - |S_{22}|^2) + |\Gamma_s|^2(|S_{11}|^2 - |\Delta|^2) - 2\,\text{Re}\,(\Gamma_s C_1)} \tag{6}$$

Taking the bilinear transformation of (7), we find that the expressions of Q and M_c should be

$$Q = |S_{21}|^2 + |S_{22}|^2 - 1$$

$$M_c = |S_{21}|^4 W(W - 4r_n(1 - |\Gamma_{\text{on}}|^2))$$

In the Section III of the paper, the authors presented the design of an experimental amplifier. In this design, some calculations are incorrect. By applying the measured S-parameters and the noise parameters of the transistor (NE 71083 GaAs FET) given by the authors into the original equations, we obtain the amplifier parameters as $K = 0.728, |\Delta| = 1.082, M_{\min} = 1.221$. Similarly, using the corrected equations, we obtain the amplifier parameters as $K = 0.728, |\Delta| = 1.082, M_{\min} = 1.006$. Both sets of parameters do not agree with the results of the paper [1]. Moreover, they will result in a potentially unstable situation.

The typical parameters of the transistor NE71083 listed in data sheet are as follows:

$$S_{11} = 0.68 \angle -173 \qquad S_{21} = 1.78 \angle 17$$

$$S_{12} = 0.09 \angle -12 \qquad S_{22} = 0.6 \angle -126$$

$$F_{\min} = 1.35\,\text{dB} \qquad \Gamma_{\text{on}} = 0.50 \angle 168$$

$$r_n = 14\,\Omega$$

which is at the conditions of $f_0 = 10$ GHz $V_{ds} = 3.0$ V and $I_{ds} = 10$ mA.

Using the corrected equations and the above parameters, we obtain as $K = 5.779|\Delta| = 0.345$ and $M_{\min} = 0.406$. Obviously, the transistor is unconditionally stable. This implies that the measured parameters of the transistor in the paper [1] might be incorrect.

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References

[1] C. R. Poole and D. K. Paul, "Optimum noise measure terminations for microwave transistor amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, no. 11, pp. 1254–1257, Nov. 1985.

Reply to Comments on "Optimum Noise Measure Terminations for Microwave Transistor Amplifiers"

D. K. Paul, P. Gardner, and C. R. Poole

The commentators' remarks refer firstly to the equations used and derived in Section II, and secondly to the experimental data in Section III of the paper [1].

Considering firstly the theoretical work in Section II, we are grateful to the commentators for correctly pointing out the errors in (5) and (6) and in the expressions for Q and M_c used in (7). Each of these errors was typographical in origin, and subsequent calculations in the paper were based on the correct equations.

We now consider the commentators' remarks on the numerical calculations in Section III.

Firstly, we maintain that our value for K, based on the measured S-parameters for the transistor, was correct, within a small rounding error. The commentators' value for K is incorrect. Secondly, we agree with the commentators that, for the measured S-parameters, $|\Delta| = 1.082$. A small discrepancy in the third decimal place was due to rounding errors. Thirdly, we agree with the commentators concerning the value of $M_{\min}$. The source of the error in the value published in the paper is not clear.

We further agree with the commentators that the transistor is potentially unstable. However we would respectfully point out that potential instability is not an uncommon situation in low noise FET amplifier design. Design rules for preventing actual instability in such cases are well established, and were employed in the design described.

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